REMARKS

Claims 1-14 are pending in the application. In the Office Action of February 4, 2003, the Examiner made the following disposition:

A.) Rejected claims 1-6 under 35 U.S.C. §112, second paragraph.

B.) Rejected claims 1, 2, and 4-6 under 35 U.S.C. §102(b) as being anticipated by "Prior Art".

C.) Rejected claims 3 and 7-14 under 35 U.S.C. §103(a) as being unpatentable over "Prior Art" in view of *Jiang et al.*

Applicants respectfully traverse the rejections and address the Examiner's disposition as follows:

A.) Rejection of claims 1-6 under 35 U.S.C. §112, second paragraph:

Claims 1-6 have been cancelled. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"VERSION WITH MARKING TO SHOW CHANGES MADE**.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

B.) Rejection of claims 1, 2, and 4-6 under 35 U.S.C. §102(b) as being anticipated by "Prior Art":

Claims 1, 2, and 4-6 have been cancelled.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

C.) Rejection of claims 3 and 7-14 under 35 U.S.C. §103(a) as being unpatentable over "Prior Art" in view of *Jiang et al.*:

Applicants respectfully disagree with the rejection.

Applicants' independent claim 7 has been amended to clarify that the entire conductive base member is removed by etching. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"VERSION WITH MARKING TO SHOW CHANGES MADE**.

Referring to Applicants' Figure 2 for illustrative purposes, claim 7 claims a method of producing an electronics parts mounting board. A circuit electrode board 20' is formed by forming a specific circuit electrode pattern 16 on a surface of one side of a conductive base member 20 to be plated and etched, by plating a specific conductive material thereon (FIGs. 2B-2D). A non-plated material 18, 19, 21 is selectively formed on the circuit electrode board 20' on which said circuit electrode pattern 16 has been formed (FIGs. 2D-2F). A projecting electrode 14 for connection is formed on the circuit electrode pattern 16 by plating a specific conductive material on said circuit electrode pattern 16 with said non-plated material 18, 19, 21 used as a mask (FIGs. 2G-2H).

After removing the non-plated material 18, 19, 21, an insulating thermal bonding member 15 is put between the circuit electrode board 20' and a specific electrode circuit base member 12, pressing the projecting electrode 14 of the circuit electrode board 20' into the thermal bonding member 15 so as to reach the electrode circuit base member 12, to bond the circuit electrode board 20' to the electrode circuit base member 12 (FIG. 2I-2J). Then, the entire conductive base member 20 is removed from a multilayer board 100 obtained by bonding the circuit electrode board 20' to the electrode circuit base member 12 by etching (not shown in FIG. 2; page 23, lines 15-16).

This is clearly unlike the "Prior Art" in view of *Jiang et al.* Referring to Applicants' FIGs 3 and 4 for a description of the "Prior Art", the "Prior Art" discloses forming bump electrodes 4' on a metal foil 2. As clearly described in Applicants' specification, the "Prior Art" bumps 4' are formed by overprinting (bump-printing) copper-containing conductive paste at specific locations on the metal foil 2. (Specification, page 6, lines 4-6). After the bumps 4' are made to contact the electrodes 2 through the resin layer 5, the metal foil 2 is selectively etched to form circuit electrodes 6. (See FIGs. 3 and 4B).

Therefore, unlike Applicants' claim 7, the "Prior Art" fails to disclose or suggest forming a circuit electrode pattern on a surface of a conductive base member and then forming projecting electrodes on the circuit electrode pattern. Instead, the "Prior Art" discloses forming projecting electrodes (bumps) 4' directly on a metal foil 2, which is later etched to become a circuit electrode pattern 6. In other words, the "Prior Art" fails to disclose or suggest Applicants' conductive base member that is different than the circuit electrode pattern.

Further, the "Prior Art" fails to disclose or suggest selectively forming a non-plated material on a circuit electrode board. As described above, the "Prior Art" discloses bump-printing bumps directly on its metal foil. Unlike claim 7, nowhere does the "Prior Art" disclose or suggest forming a non-plated material on its metal foil.

Accordingly, since the "Prior Art" fails to disclose or suggest a non-plated material, the "Prior Art" could neither disclose nor suggest using a non-plated material as a mask or removing a non-plated material.

Also, since the "Prior Art's" metal foil 2 is selectively etched to form circuit electrodes 6 and is not equivalent to Applicants' conductive base member, the "Prior Art" could not disclose or suggest removing an <u>entire</u> conductive base member from a multilayer board obtained by bonding a circuit electrode board to a electrode circuit base member by etching.

Therefore, the "Prior Art" alone fails to disclose or suggest many claimed elements of claim 7.

The "Prior Art" in view of *Jiang et al.* still fails to disclose or suggest claim 7. *Jiang et al.* discloses forming a circuit electrode pattern 12 on a dielectric layer 11. (*Jiang et al.*, Figure 1). Additional layers 14 and 16 are then applied on top of the dielectric layer 11. (*Jiang et al.*, Figure 2). Apertures 18 are formed through the layers 11, 14, 16 and a conductive material 20 is filled in the apertures 18. (*Jiang et al.*, Figures 3-4).

Thus, unlike Applicants' claim 7, *Jiang et al.* still fails to disclose or suggest forming a circuit electrode pattern on a conductive base member. Instead, *Jiang et al.* forms its conductive electrode pattern on a dielectric member. Also, unlike Applicants' claim 7 that removes the non-plated material after forming projecting electrodes, *Jiang et al.* merely forms non-plated layers 11, 14, 16 and then fails to remove them. *Jiang et al.'s* conductive material 20 is left as conductors within the apertures 18 in the layers 11, 14, 16 instead of as projecting electrodes.

Further, since *Jiang et al.* fails to disclose or suggest a conductive base member, *Jiang et al.* still fails to disclose or suggest removing an entire conductive base member from a multilayer board obtained by bonding a circuit electrode board to a electrode circuit base member by etching.

As clearly described above, the "Prior Art" and *Jiang et al.*, taken singly or in combination, fail to disclose or suggest many claimed elements of claim 7. Therefore, Applicants respectfully submit claim 7 is allowable over the cited references.

Claims 8-14 depend directly from claim 7 and therefore allowable for at least the same reasons that claim 7 is allowable.

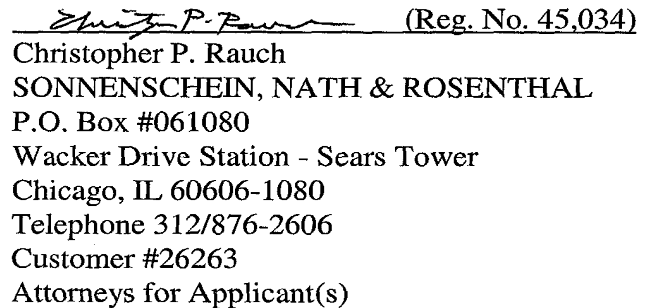
Claim 3 has been canceled.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

CONCLUSION

In view of the foregoing, it is submitted that claims 7-14 are patentable. It is therefore submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please cancel claims 1-6.

Please amend claim 7 as follows:

7. (Amended) A method of producing an electronics parts mounting board, comprising the steps of:

forming a circuit electrode board by forming a specific circuit electrode pattern on a surface of one side of a conductive base member to be plated and etched, by plating a specific conductive material thereon;

selectively forming a non-plated material on said circuit electrode board on which said circuit electrode pattern has been formed;

forming a projecting electrode for connection on said circuit electrode pattern by plating a specific conductive material on said circuit electrode pattern with said non-plated material used as a mask;

after removing said non-plated material, putting an insulating thermal bonding member between said circuit electrode board and a specific electrode circuit base member, pressing said projecting electrode of said circuit electrode board into said thermal bonding member so as to reach said electrode circuit base member, to bond said circuit electrode board to said electrode circuit base member; and

removing said entire conductive base member from a multilayer board obtained by bonding said circuit electrode board to said electrode circuit base member by [selective] etching.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited as First Class Mail in an envelope addressed to Asst. Commissioner for Patents, Washington, D.C. 20231 on April 15, 2003.

(Reg. No. 45,034)
Christopher P. Rauch